A Step-up Multilevel Inverter Topology using Novel Switched Capacitor Converters with Reduced Components

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***Abstract*— In this paper, basic cell (BC) of a novel switched capacitor converter (SCC) has been proposed first. After that, the generalized structure of proposed SCC is developed. The developed SCC requires reduced number of switches, drivers, diodes, capacitors and lower number of conducting switches in current flow paths and capacitor charging paths as compared to the other recently developed SCCs. A switched capacitor multilevel inverter (SCMLI) utilizing 2 number of generalized SCCs is developed next. Further, cascaded extension of proposed SCMLI is realized and analyzed for symmetric and asymmetric dc source configurations. A detail analysis of optimum selection of capacitance for switched capacitors of 13 level SCMLI is presented. An extensive comparison study shows that the proposed SCMLI requires lower number of components as compared to other SCMLIs. Further, the proposed structure has minimum cost function per level per boosting factor as compared to the other SCMLIs. Extensive experimental results considering fundamental switching frequency scheme are presented to validate the merits and effectiveness of the proposed structure.**

***Index Terms*— Boosting factor, multilevel inverter, switched capacitor, reduced devices, voltage balance**

I. INTRODUCTION

IN recent years, multilevel inverters (MLIs) have become a viable dc to ac power conversion system for different applications such as renewable energy conversion systems, motor drive applications, UPS systems, FACTs applications, induction heating systems, distributed generation systems etc [**1-4**]. As compared to classic 2-level inverters, MLIs have numerous advantages such as (1) they can handle high power level using medium voltage rated semiconductor devices, (2) they can produce output voltage waveform with better harmonic spectrum, (3) they are sustained by lower electromagnetic interfaces (EMIs) and lower dv/dt stresses and (4) they have higher efficiency [**5**].

Generally, conventional MLIs are categorized into three types: neutral point clamped (NPC) MLI, flying capacitor (FC) MLI and cascaded H-bridge (CHB) MLI. Conventional MLIs become very popular in different industrial applications for generating a specific output voltage level (up-to 5 levels) [**6-7**]. However, they require large number of components for producing higher level output voltage waveform. NPC-MLI requires large number of dc link capacitors and clamping diodes, FC-MLI requires large number of flying capacitors and CHB-MLI requires large number of isolated dc power supplies. Further, NPC and FC MLIs suffer from capacitor voltage unbalancing problem. In addition, conventional MLIs do not possess inherent output voltage boosting ability (i.e. self-boosting ability) which is desirable for boosting the low output voltage of renewable sources such as photovoltaic array to desired load or grid voltage level.

In recent years, a significant research interest among researchers is found in topological development of MLI structures and in solving the capacitor voltage unbalancing problem. A number of reduced device count MLIs have been proposed in recent years [**8-9**]. However, these structures do not have self-boosting ability. By incorporating front-end dc to dc converters [**10**] or impedance networks [**11-12**], large number of topologies have been proposed to add boosting feature to conventional MLIs. However, magnetic elements present in these topologies make power circuit bulky and less efficient. A number of auxiliary circuits[**13**] or complex control algorithms [**14**] have been proposed to mitigate the capacitor voltage unbalancing problem. However, these methods enhance size, cost and complexity of the inverter structure.

Switched capacitor MLI (SCMLI) is a special kind of MLIs which can produce a boosted sinusoidal output voltage by using reduced number of power supplies. SCMLI uses capacitors as alternate dc sources. Further, SCMLI does not require any auxiliary circuits or complex control algorithms to balance the capacitor voltages. Mac and Ionovici introduced the concept of SCMLI in the year of 1998 [**15**].

In recent years, numerous number of innovative SCMLIs have been reported in literature [**16-27**]. Hinago and Koizumi proposed a novel SCMLI structure in [**16**]. The structure requires large number of switches, capacitors and needs to conduct large number of switches for generating highest

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output voltage (i.e. N_{path} is high) and to charge the capacitors (i.e. N_{path_C} is high) when output voltage level enhances. High value of N_{path} and N_{path_C} degrade the quality of output voltage waveform and reduce the peak amplitude of output voltage (this is happened due to on-state voltage drops in conducting switches). Further, the structure requires an H-bridge circuit for polarity generation which enhances total standing voltage (TSV) of the structure. A switched capacitor basic cell (SCBC) consisting of 2 switches, 1 diode and 1 capacitor was proposed by Babaei and Gowgani [**17**]. Based on these SCBCs, 2 number of SCMLI structures have been developed in [**17**]. However, the structures have H-bridge circuits and require large number of switches and N_{path} for producing high quality output voltage waveform. To reduce the number of switches, Ye et. al. proposed a SCMLI in [**18**]. However, the structure requires H-bridge circuit, large number of power diodes, capacitors and high value of N_{path} and N_{path_C}. A cascaded SCMLI for high frequency ac power system was proposed by Liu et. al. in [**19**]. Each module of proposed structure requires H-bridge circuit which enhances number of components, TSV and N_{path} of the structure. Zamiri et. al. proposed a novel switched capacitor converter (SCC) first [**20**]. After that, a SCMLI structure consisting of 2 number of SCCs was proposed. Further, cascaded SCMLI was developed. However, the structure has the problem of high TSV and requires large number of dc sources, capacitors, N_{path} and N_{path_C} for producing higher level output voltage waveform. A generalized structure of SCMLI based on the same SCC as proposed in [**20**] by Barzegarkhoo et.al. in [**21**]. The proposed structure cannot sum all dc sources at a time which limits its dc source utilization factor as well as reduces boosting factor and output voltage level generation. Saeedian et. al. proposed a step-up MLI structure based on SC technique in [**22**]. Each module of the proposed structure can produce 5 output voltage levels. In this structure, all capacitors cannot be connected in series with input source at a time. This limits boosting factor as well as output voltage level generation of the structure. A new boost SCMLI was proposed by Barzegarkhoo et. al. in [**23**]. The proposed structure can produce higher number of voltage levels as compared to others. However, the capacitors utilized in this structure cannot be charged to full dc link voltage which limits its boosting factor. Further, the structure requires large number of switches, capacitors and dc sources when high output voltage level is intended to produce. A cross-switched MLI using novel SCCs was developed by Roy et. al. in [**24**]. The proposed structure requires lower switches and TSV as compared to others. However, the structure is not modular in nature and the structure requires significantly large number of switches, capacitors and N_{path} for producing high quality output voltage. A 5 level SCMLI and its cascaded extension were proposed by Saeedian et. al. [**25**]. The structure cannot add all capacitor voltages with the input source which limits its boosting factor as well as output voltage level generation. Further, N_{path_C} is higher than others which degrades capacitor voltage and output voltage profiles. Liu et.al. proposed a 7 level SCMLI and its cascaded structure in [**26**]. Although the structure sustains lower voltage stresses, the structure cannot add all capacitors with the input source which limits its boosting factor and output voltage level. In cascaded form, the proposed structure requires significantly large number of capacitors without enhancing boosting factor of the structure. Peng et. al. proposed a 7 level SCMLI in [**27**]. Further, a cascaded structure was developed. The structure provides higher boosting factor as compared to others. However, the structure requires H-bridge circuit and requires significantly large number of switches, power diodes, capacitors and N_{path} for producing high quality output voltage waveform.

It is observed that the major drawbacks of SCMLIs are (1) they require significantly large number of components for producing higher level output voltage waveform, (2) the lower boosting factor of the structures, (3) the large number of N_{path} and N_{path_C} which degrade the quality of output voltage waveform, and (4) high TSV of the structures. Hence, there has a research scope to develop SCMLI structure which requires lower components, N_{path} and N_{path_C}, provides higher boosting factor and lower TSV. Nevertheless, there has a trade-off between the number of components and TSV of the structure at same boosting factor.

In this paper, a novel SCC structure and its extended form are presented first. The proposed SCC has the advantage of minimum and constant N_{path} and N_{path_C} as compared to other SCCs whenever the output voltage level of SCC enhances. Further the SCC requires lower number of components as compared to other SCCs. After that a SCMLI and its cascaded extension are presented. The SCMLI structure requires lower number of components, N_{path} and N_{path_C} as compared to the recently developed SCMLIs. Detail operating principle, switched capacitor selection procedure have been presented in depth. Cost function comparison among the topologies have been presented. Finally, extensive experimental results are provided to validate the merits and effectiveness of the proposed structure.

II. Basic Cell of Proposed SCC

Basic Cell (BC) of the proposed SCC is depicted in Fig. 1(a). It comprises of 4 switches (S_1, S_2, S_{1c} and S_{2c}), 1 diode (D), 2 capacitors (C_1 and C_2) and 1 dc power supply (V_{in}). Switches S_2, S_{1c} and S_{2c} do not have anti-parallel diode whereas switch S_1 has anti-parallel diode. Capacitors C_1 and C_2 can be charged up-to V_{in} by connecting them in parallel with V_{in} individually by applying appropriate switching states. With these capacitor voltages, BC can produce 3 positive voltage levels ($+V_{in}$, $+2V_{in}$ and $+3V_{in}$) across output terminals A and B. Table I shows state of the switches and capacitors corresponding to different output voltage levels. Where '1' and '0' stand for on and off states of switches respectively. Further, charging state, discharging state and not-connected state of the capacitors are indicated by 'C', 'D' and 'NC' respectively.

Fig. 1(b) shows equivalent circuit and current flow paths when S_{2c} is on. During this switching state, C_2 is connected in parallel with V_{in} through D. Hence, C_2 accumulates energy from V_{in} and is charged near about V_{in}. Charging current for C_2 is i_{C2} as shown in Fig. 1(b). Whereas C_1 remains in NC state.

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Further, during this switching state, output voltage of BC (i.e. v_{AB}) is equal to V_{in}.

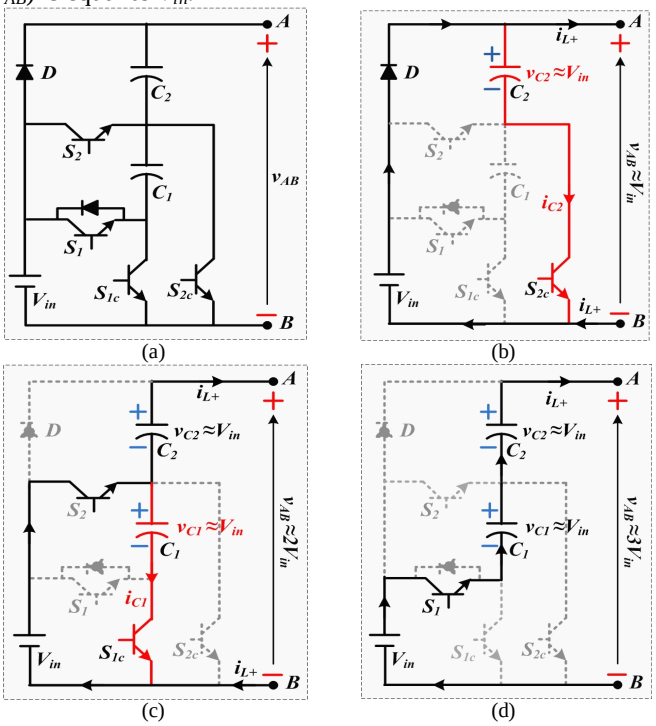

Fig.1. Figure presents (a) BC of proposed SCC; Equivalent circuit and current flow paths of proposed BC when v_{AB} is (b) $+V_{in}$, (c) $+2V_{in}$ and (d) $+3V_{in}$

Fig. 1(c) depicts equivalent circuit and current flow paths when S_2 and S_{1c} are turned on. With this switching state, C_1 is connected in parallel with V_{in} whereas C_2 is connected in series with V_{in}. Hence, C_1 accumulates energy from V_{in} whereas C_2 transfers its stored energy towards the load. During this switching state, v_{AB} is equal to summation of V_{in} and voltage across C_2 i.e. v_{AB} is nearly equal to $2V_{in}$. The charging current for C_1 is i_{C1} as depicted in Fig. 1(c).

When S_1 is turned on, both C_1 and C_2 are connected in series with V_{in}. Hence, output voltage of BC is equal to near about $3V_{in}$. In this state, both capacitors are in discharging state and transfer their stored energy towards the load as depicted in Fig. 1(d) and Table I.

TABLE I
SWITCH AND CAPACITOR STATES FOR BASIC CELL

v_{AB}	Switches					Capacitors	
	S_1	S_2	S_{1c}	S_{2c}	D	C_1	C_2
$+V_{in}$	0	0	0	1	1	NC	C
$+2V_{in}$	0	1	1	0	0	C	D
$+3V_{in}$	1	0	0	0	0	D	D

From this above discussion, it can be concluded that (a) the proposed BC has self- boosting ability ; boosting factor i.e. the ratio of peak output of BC and input dc source, is equal to 3, (b) the capacitors can be connected in series/parallel with input supply using simple switching strategy and at the same time output voltage level can be produced, (c) by turning on only one switch (S_1), the highest output voltage level (i.e. $+3V_{in}$) can be produced. (d) stress voltages for S_1, S_2, S_{1c} and S_{2c} are $2V_{in}$, V_{in}, V_{in} and $2V_{in}$ respectively. Hence, TSV of the BC is $6V_{in}$. Further, peak inverse voltage (PIV) of the diode D is $2V_{in}$.

III. GENERALIZED STRUCTURE OF PROPOSED SCC

This section presents the development of generalized structure of proposed SCC. The structure is developed by connecting n number of capacitors (C_1 to C_n) in series connection as shown in Fig. 2. A switch S_{ic} (i =1 to n) is connected between negative terminal of C_i (i=1 to n) and negative terminal of V_{in}. Similarly, a switch S_i (i=2 to n) is connected between mid-point of 2 capacitors C_i and $C_{(i-1)}$ (i=2 to n) and positive terminal of V_{in} as shown in Fig. 2. Switch S_1 is connected in between positive terminal of V_{in} and negative terminal of C_1.

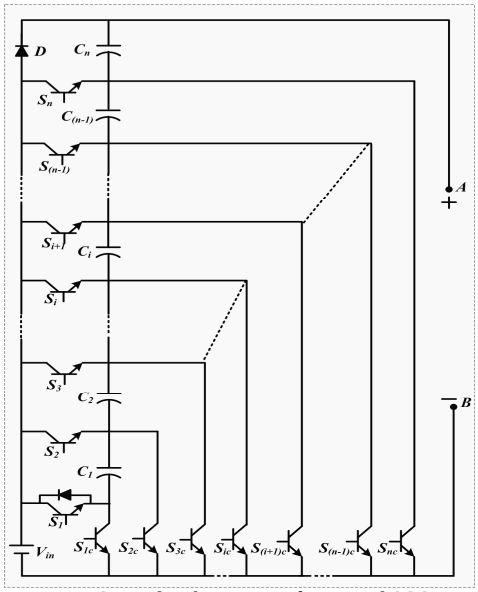

Fig.2. Generalized structure of proposed SCC

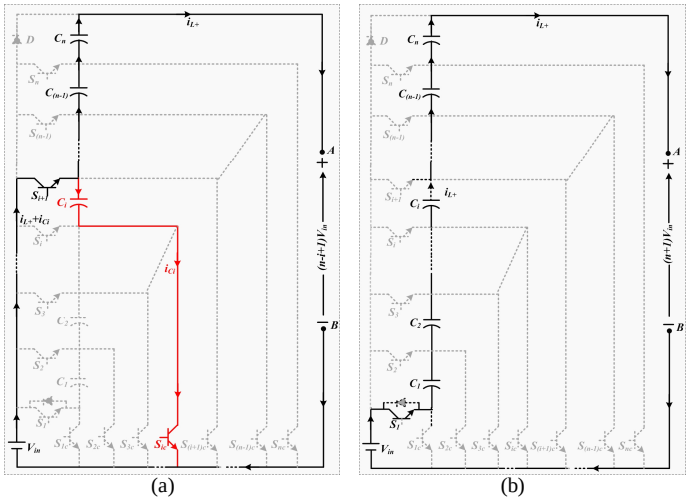

Fig.3. Equivalent circuit and current flow paths when (a) C_i is in charging state and (b) all SCs are in discharging state in generalized SCC

All the capacitors in this structure can be charged to V_{in} by turning on appropriate switches. For example, i^{th} capacitor, C_i can be charged to V_{in} by turning on switches S_{i+1} and S_{ic} as shown in Fig. 3(a). During this switching state, the generated

output voltage appeared across A to B is $(n\text{-}i\text{+}1)V_{in}$. Capacitors connected above of C_i i.e. (C_n to $C_{n\text{-}i}$) are in discharging state whereas capacitors connected to lower of C_i i.e. (C_1 to $C_{i\text{-}1}$) are in NC state. It is observed that the structure needs to conduct only 2 switches to charge any utilized capacitors. Hence, N_{path_C} for the SCC (i.e. $N_{path\_C\_scc}$) is 2 and it does not depend on n.

When S_1 is turned on and other switches are in off condition, all the capacitors are connected in series with V_{in} and highest voltage level of SCC i.e. $(n\text{+}1)V_{in}$ is generated across A to B as shown in Fig. 3(b). During this switching state, all capacitors are in discharging state. As the structure needs to conduct only 1 switch to produce the highest voltage level, N_{path} for the SCC (i.e. N_{path_scc}) is 1 and it is independent of n.

The number of switches (N_{sw_scc}), drivers (N_{dr_scc}), capacitors (N_{cap_scc}) and TSV (TSV_SCC) of generalized SCC in terms of n can be expressed by (1)-(3). The structure requires only one power diode (i.e. N_{dio_scc}=1).

$$N_{sw\_scc} = N_{dr\_scc} = 2n \tag{1}$$

$$N_{cap\_scc} = n \tag{2}$$

$$TSV\_SCC = \begin{cases} \frac{1}{4}(5n^2+2n+1) & \forall\ n = \text{odd} \\ \frac{1}{4}(5n^2+2n) & \forall\ n = \text{even} \end{cases} \tag{3}$$

IV. Comparison of Proposed SCC with other SCCs

This section presents the comparison of proposed BC and generalized structure of SCC with the recently developed SCCs presented in [**15-17, 20-21, 23, 24**].

A. Comparison of proposed BC with others

Table II shows the comparison of proposed BC with other SCCs in respect of component requirement, boosting factor (B_{scc}) and ($TSV\text{+}PIV$). As per Table II, the proposed BC requires lower number of switches and drivers as compared to the SCCs presented in [**15-16, 23-24**]. The switch per level (N_{sw_scc}/N_{L_scc}) for proposed BC is 1.33 which is lower than the SCCs presented in [**15-16, 23-24**] as shown in Table II. The SCC presented in [**17**] requires same number of switches and drivers as that for proposed one. However it requires more number of power diodes. The proposed BC has higher B_{scc} than SCC presented in [**23**]. B_{scc} for [**23**] is 2 whereas that for proposed BC is 3. The is due to inability of the SCC presented in [**23**] to charge the capacitors up-to the full dc supply voltage.

The SCC presented in [**20-21**] requires lower number of switches as compared to the proposed BC. As per Table II, N_{sw_scc}/N_{L_scc} for [**20-21**] is 1.25 whereas that for proposed BC is 1.33. However, the SCC presented in [**20-21**] requires two capacitors of different voltage ratings. The maximum voltage rating of utilized capacitors (V_{Cmax_rating}) for [**20-21**] is $2V_{in}$ whereas the proposed BC utilizes two capacitors of equal voltage rating as shown in Table II. Each capacitor voltage rating of proposed BC is V_{in}. This can reduce the cost of the capacitors of proposed BC as compared to the SCC presented in [**20-21**].

The major advantage of proposed BC is that it requires lower N_{path_scc} than others. As per Table II, N_{path_scc} of proposed BC is 1 whereas N_{path_scc} for [**15-17, 20-21, 24**] is 2. Further, it can be observed that the proposed BC requires minimum $N_{path\_C\_scc}$ as compared to the structures presented in [**15-17, 20-21, 24**]. However, the proposed BC sustains more ($TSV\text{+}PIV$) as compared to the SCCs in [**16-17, 20-21, 23-24**].

TABLE II
COMPARISON OF PROPOSED BASIC CELL OF SCC WITH OTHER SCCS

Parameters	SCC presented in (n=2)						
	[15] 1998	[16] 2012	[17] 2014	[20-21] 2016	[23] 2018	[24] 2019	Proposed BC
N_{L_scc}	3	3	3	4	4	3	3
N_{sw_scc}	5	6	4	5	7	5	4
N_{dr_scc}	5	6	4	5	5	5	4
N_{dio_scc}	3	-	2	1	1	-	1
N_{cap_scc}	2	2	2	2	2	2	2
N_{path_scc}	3	2	2	2	1	2	1
$N_{path\_C\_scc}$	3	4	4	3	2	3	2
B_{scc}	3	3	3	4	2	3	3
N_{sw_scc}/N_{L_scc}	1.67	2	1.33	1.25	1.75	1.67	1.33
V_{Cmax_rating}	V_{in}	V_{in}	V_{in}	$2V_{in}$	V_{in}	V_{in}	V_{in}
$(TSV\text{+}PIV)_{scc}$	$8V_{in}$	$6V_{in}$	$6V_{in}$	$9V_{in}$	$5V_{in}$	$5V_{in}$	$8V_{in}$

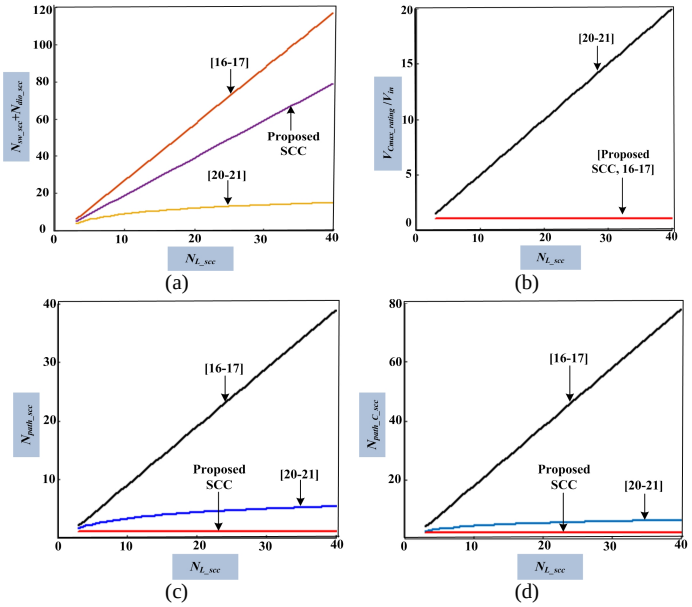

Fig.4. Variation of required (a) semiconductor devices, (b) V_{Cmax_rating}/V_{in} (c) N_{path_scc} and (d) $N_{path\_C\_scc}$ with respect to N_{L_scc} for proposed SCC and the SCCs presented in [**16**, **17**, **20-21**]

B. Comparison of generalized SCC with other SCCs

Fig. 4 shows the comparison of proposed generalized SCC with others generalized SCCs presented in [**16, 17, 20-21**]. Fig. 4(a) depicts the variation of required semiconductor devices (i.e. $N_{sw\_scc}\text{+}N_{dio\_scc}$) with respect to output voltage level of SCC (N_{L_scc}). From this figure, it can be observe that the proposed SCC requires lower number of semiconductor devices as compared to the SCCs presented in [**16-17**] for producing a N_{L_scc}. As compared to the SCC presented in [**20-21**], the proposed SCC requires higher number of semiconductor devices for producing a N_{L_scc}. However, the SCC presented in [**20-21**] requires different voltage rated capacitors for producing a N_{L_scc} whereas the proposed SCC requires same voltage rated capacitors. As shown in Fig. 4(b), the highest capacitor voltage rating (V_{Cmax_rating}) per V_{in} for the SCC presented in [**20--21**] increases linearly with the

TABLE III
SWITCH AND CAPACITOR STATES FOR PROPOSED 13 LEVEL SCMLI IN POSITIVE HALF CYCLE

$\frac{v_o}{V_{dc}}$	on switches during the first quarter cycle	C_{11}	C_{21}	C_{12}	C_{22}	on switches during the second quarter cycle	C_{11}	C_{21}	C_{12}	C_{22}
+6	$S_{U1}, S_{11}, S_{L2}, S_{12}, S_{U3}$	D	D	D	D	$S_{U1}, S_{11}, S_{L2}, S_{12}, S_{U3}$	D	D	D	D
+5	$S_{U1}, S_{21}, S_{L2}, S_{12}, S_{U3}, S_{1c1}$	C	D	D	D	$S_{U1}, S_{11}, S_{L2}, S_{22}, S_{U3}, S_{1c2}$	D	D	C	D
+4	$S_{U1}, S_{2c1}, S_{L2}, S_{12}, S_{U3}$	NC	C	D	D	$S_{U1}, S_{11}, S_{L2}, S_{2c2}, S_{U3}$	D	D	NC	C
+3	$S_{U1}, S_{21}, S_{1c1}, S_{L2}, S_{2c2}, S_{U3}$	C	D	NC	C	$S_{U1}, S_{2c1}, S_{L2}, S_{22}, S_{1c2}, S_{U3}$	NC	C	C	D
+2	$S_{U1}, S_{2c1}, S_{L2}, S_{2c2}, S_{U3}$	NC	C	NC	C	$S_{U1}, S_{2c1}, S_{L2}, S_{2c2}, S_{U3}$	NC	C	NC	C
+1	$S_{U1}, S_{2c1}, S_{L2}, S_{L3}, S_{22}, S_{1c2}$	NC	C	C	NC	$S_{L1}, S_{L2}, S_{2c2}, S_{U3}, S_{21}, S_{1c1}$	C	NC	NC	C
0	$S_{U1}, S_{U2}, S_{U3}, S_{21}, S_{1c1}, S_{22}, S_{1c2}$	C	NC	C	NC	$S_{L1}, S_{L2}, S_{L3}, S_{22}, S_{1c2}, S_{21}, S_{1c1}$	C	NC	C	NC

increment of N_{L_scc} whereas that for proposed SCC remains constant with respect to N_{L_scc}. This reduces the capacitor cost of the proposed SCC as compared to the SCC presented in [**20-21**].

Fig. 4(c) shows the variation of N_{path_scc} with respect to N_{L_scc} for proposed and suggested topologies. It can be observed that the proposed SCC has a minimum and constant N_{path} in respect of N_{L_scc}. This improves the peak magnitude of output voltage as minimum switches need to conduct (hence lower voltage drops) in current flow path for producing highest voltage level. Fig. 4(d) shows the variation of $N_{path\text{-}C\text{-}scc}$ with respect to N_{L_scc}. It can be observed that the proposed SCC requires minimum and constant $N_{path\_C\_scc}$ as compared to other SCCs. This feature of proposed SCC improves the capacitor voltage profiles as well as the output voltage waveform. This is the major advantage of the proposed SCC as compared to the other SCCs.

V. PROPOSED SCMLI AND ITS CASCADED EXTENSION

This section presents the proposed SCMLI and its cascaded extension. Fig. 5 shows the proposed SCMLI consisting of 2 proposed SCCs (*SCC 1* and *SCC 2*), 2 legs (*Leg 1* and *Leg 2*) and 1 link (*Link*) circuit. The proposed structure comprises of 2 number of dc sources V_{in1} and V_{in2}, 2n number of capacitors, 2 number of diodes, (4n+6) number of switches and drivers. *Leg1*, *Link* and *Leg 2* consist of switches (S_{U1}, S_{L1}), (S_{U2}, S_{L2}) and (S_{U3}, S_{L3}) respectively. v_{o1} and v_{o2} are output voltages of *SCC 1* and *SCC 2* respectively. The maximum voltage generated by *SCC 1* and *SCC 2* are (n+1)V_{in1} and (n+1) V_{in2}. Hence, the maximum voltage produced by the proposed SCMLI is (n+1)(V_{in1}+V_{in2}).

The proposed SCMLI with n=2 is depicted in Fig. 6. C_{11} and C_{21} are the capacitors for *SCC 1* whereas C_{12} and C_{22} are the capacitors for *SCC 2*. When both the input sources are equal in magnitude (i.e. V_{in1}=V_{in2}=V_{dc}), the proposed structure (n=2) can produce 13 output voltage levels. The list of on switches and capacitor states for positive half-cycle of 13 level output voltage are shown in Table III. In this table, the on switches and capacitor states are shown for quarter cycles present in positive half-cycle. As negative half-cycle of output voltage is symmetrical to positive half cycle, the capacitor states and switching states of SCCs remain similar in negative half-cycle as that for positive half-cycle. However, in negative half-cycle, polarity of output voltage can be reversed across load by turning on the complementary switches present in *Leg 1*, *Leg 2* and *Link* circuits. Similarly, for n=2, the proposed structure can produce 31 output voltage levels with asymmetric dc sources (V_{in1}=V_{dc} and V_{in2}=4V_{dc}).

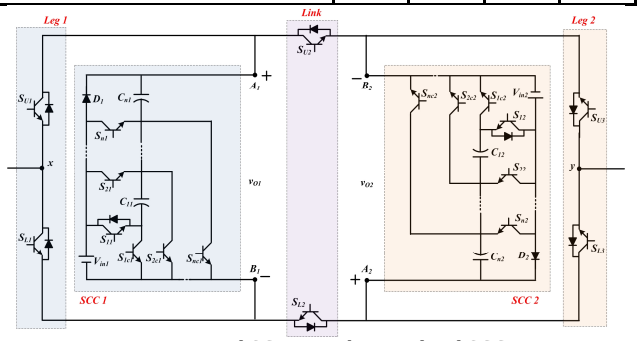

Fig.5. Proposed SCMLI with generalized SCCs

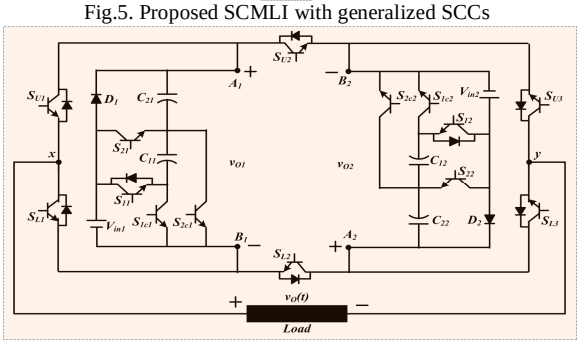

Fig.6. Proposed SCMLI with n=2

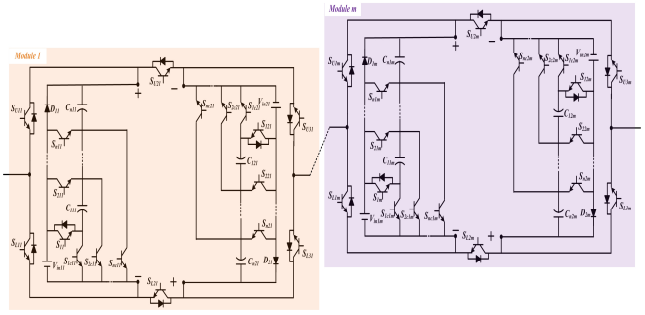

Fig.7. Cascaded extension of proposed SCMLI

The cascaded extension of proposed SCMLI is shown in Fig. 7. It consists of m number of modules. The required switches (N_{sw}) and drivers (N_{dri}), capacitors (N_{cap}), diodes (N_{dio}), dc sources (N_{dc}), N_{path} and N_{path_C} can be expressed by (4) and (5).

$$N_{sw} = N_{dr} = (4n+6)m \;;\; N_{cap} = 2nm \tag{4}$$

$$N_{dc} = N_{dio} = 2m \;;\; N_{path} = 5m \;;\; N_{path\_C} = 2 \tag{5}$$

The cascaded SCMLI is analyzed for symmetric and asymmetric dc source configurations. In symmetric configuration, all modules have same magnitude of dc sources as presented by (6). The output voltage level and TSV of the structure can be presented by (7) and (8) respectively.

$$V_{in1k} = V_{in2k} = V_{dc} \quad \forall \ k = 1 \text{ to } m \tag{6}$$

$$N_L = 4nm + 4m + 1 \tag{7}$$

$$TSVpu_{symcas} = \frac{5n^2 + 18n + 17}{4(n+1)} \ \forall \ n = \text{odd} \ ; \quad \frac{5n^2 + 18n + 16}{4(n+1)} \ \forall \ n = \text{even} \tag{8}$$

Further, the proposed cascaded SCMLI is analyzed for asymmetric dc source configuration. In this configuration, magnitude of dc sources, generated output voltage levels and TSV of the proposed structure are presented by (9), (10) and (11) respectively.

$$V_{in1k} = (2n^2 + 8n + 7)^{k-1} V_{dc}$$

$$V_{in2k} = (n+2)(2n^2 + 8n + 7)^{k-1} V_{dc} \ \forall \ k = 1 \text{ to } m \tag{9}$$

$$N_L = (2n^2 + 8n + 7)^m \tag{10}$$

$$TSV_{puasymcas} = \frac{5n^3 + 33n^2 + 71n + 51}{4(n^2 + 4n + 3)} \ \forall \ n = \text{odd} \ ; \quad \frac{5n^3 + 33n^2 + 70n + 48}{4(n^2 + 4n + 3)} \ \forall \ n = \text{even} \tag{11}$$

VI. Selection Procedure of Capacitance for Switched Capacitors

This section presents the capacitor selection procedure for 13 level proposed SCMLI for resistive and resistive-inductive load conditions. Based on Table III and Fig. 8, longest discharging time (LDT) for C_{11} and C_{12} are same. Similarly, LDTs for C_{21} and C_{22} are same. For resistive load (R_L), the amount of charge discharged during LDTs for C_{11} and C_{12} (i.e. $\Delta Q_{C11,C12}$) and for C_{21} and C_{22} (i.e. $\Delta Q_{C21,C22}$) are presented by (12) and (13) respectively [**24**].

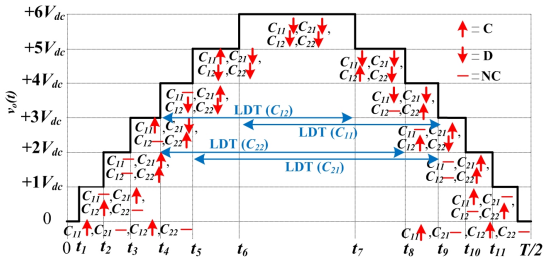

Fig.8. LDTs for SCs for 13level proposed SCMLI

$$\Delta Q_{C11,C12} = \frac{V_{dc}}{R_L}\left[4(t_5 - t_4) + 5(t_6 - t_5) + 6(t_7 - t_6)\right] \tag{12}$$

$$\Delta Q_{C21,C22} = \frac{V_{dc}}{R_L}\left[4(t_5 - t_4) + 5(t_6 - t_5) + 6(t_7 - t_6) + 5(t_8 - t_7)\right] \tag{13}$$

The times t_4, t_5, t_6, t_7 and t_8 for fundamental switching frequency scheme can be evaluated by (14).Where T and f are the time period and frequency of output voltage waveform. Similarly for resistive-inductive (R-L) load condition, the amount of charge discharged during LDTs for the SCs are presented by (15) and (16).

$$t_4 = \frac{\sin^{-1}(7/12)}{2\pi f}; t_5 = \frac{\sin^{-1}(9/12)}{2\pi f}; t_6 = \frac{\sin^{-1}(11/12)}{2\pi f}; \quad t_7 = (\frac{T}{2} - t_6); \ t_8 = (\frac{T}{2} - t_7) \tag{14}$$

$$\Delta Q_{C11,C12} = \frac{i_{L\max}}{2\pi f}\left[\cos(2\pi f t_4 - \phi) - \cos(2\pi f t_7 - \phi)\right] \tag{15}$$

$$\Delta Q_{C21,C22} = \frac{i_{L\max}}{2\pi f}\left[\cos(2\pi f t_4 - \phi) - \cos(2\pi f t_8 - \phi)\right] \tag{16}$$

Where ϕ is power factor angle of load. The optimum capacitance for C_{11}, C_{12}, C_{21} and C_{22} for a specified capacitor voltage ripple (kV_{dc}) can be presented by (17).

$$C_{11} = C_{12} \geq \frac{\Delta Q_{C11,C12}}{kV_{dc}}; \ C_{21} = C_{22} \geq \frac{\Delta Q_{C21,C22}}{kV_{dc}} \tag{17}$$

The variation of optimum capacitance for SCs for R_L and R-L load conditions are depicted in Fig. 9(a)-9(b) and 9(c)-9(d) respectively. From Fig. 9(a) and 9(b), it can be observed that capacitance for SC decreases with increasing value of R_L and k. From Fig. 9(c) and 9(d) (this figure is drawn considering 3.2A peak load current and V_{dc}=30V) , it can be observed that when ϕ and k increase, the optimum capacitance for SC decreases.

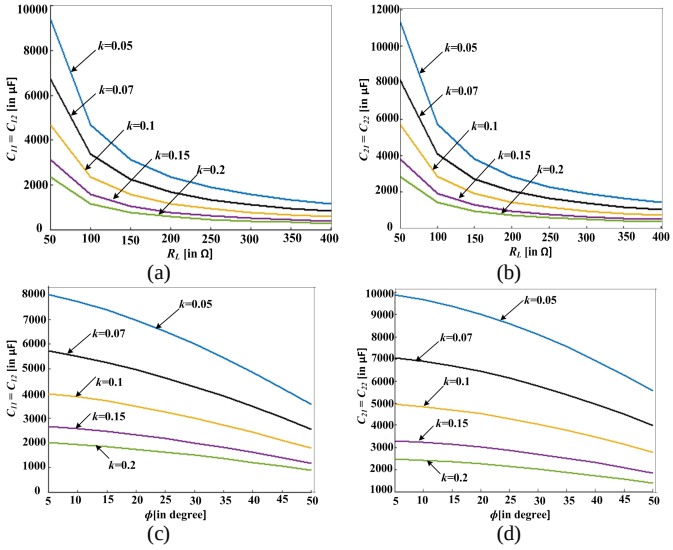

Fig. 9. Variation of optimum capacitance for (a) C_{11} and C_{12} (b) C_{21} and C_{22} for resistive load (R_L) and (c) C_{11} and C_{12} (b) C_{21} and C_{22} for different phase angles (ϕ) for different percentage of capacitor voltage ripples (k)

VII. Analysis of Power Losses for Proposed 13 Level SCMLI

This section presents the analysis of power losses for the proposed 13 level SCMLI. The major power losses associated with the structure are conduction losses (P_{con}), switching losses (P_{sw}) and capacitor voltage ripple losses (P_{rip}) [**20**]. The analysis of different losses considering fundamental switching frequency scheme are described in following sub-sections.

A. Analysis of conduction losses

The ohmic losses occurred in the internal resistances of different components associated with the structure are called

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conduction losses. The conduction losses are evaluated based on resistive load (R_L) condition as this load condition causes the worst value of conduction losses. For simplicity, it is assumed that (i) all switches with anti-parallel diode have same on-state resistance (r_{on1}) and all switches without anti-parallel diode have same on-state resistance (r_{on2}) (ii) all SCs have same equivalent series resistance (r_e) and same

TABLE IV
DIFFERENT EQUIVALENT CIRCUITS FOR PROPOSED 13 LEVEL SCMLI

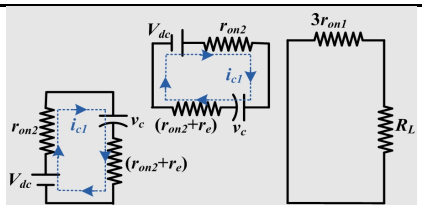
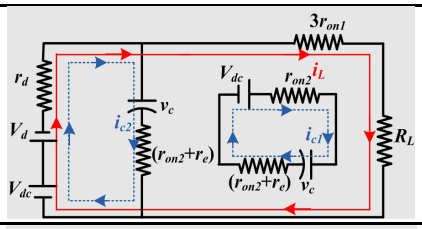
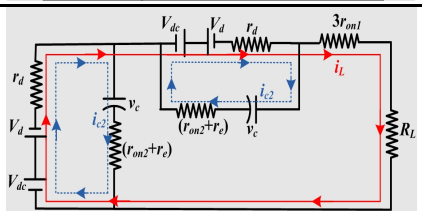
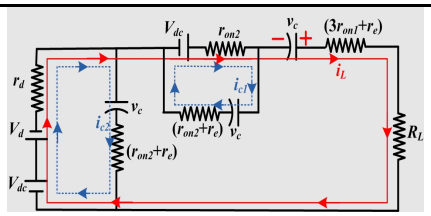
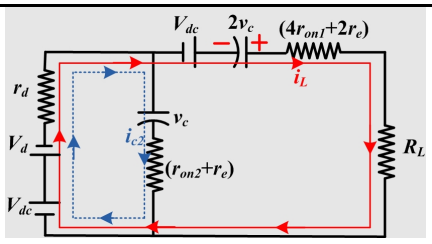
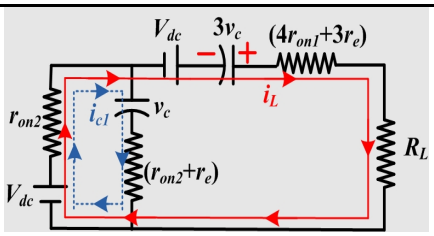
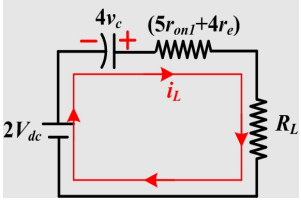
EC 0 (corresponds to ± 0)	
EC 1 (corresponds to $\pm 1V_{dc}$)	
EC 2 (corresponds to $\pm 2V_{dc}$)	
EC 3 (corresponds to $\pm 3V_{dc}$)	
EC 4 (corresponds to $\pm 4V_{dc}$)	
EC 5 (corresponds to $\pm 5V_{dc}$)	
EC 6 (corresponds to $\pm 6V_{dc}$)	

TABLE V
EXPRESSION FOR LOAD CURRENT AND CAPACITOR CURRENTS IN DIFFERENT EQUIVALENT CIRCUITS OF PROPOSED 13 LEVEL SCMLI

EC 0	$i_L = 0\ ;\ i_{C1} = \dfrac{V_{dc} - v_C}{(2r_{on2} + r_e)}\ ;\ i_{C2} = 0$
EC 1	$i_L = \dfrac{v_C(r_{on2} + r_d + r_e) + (V_{dc} - V_d - v_C)(r_{on2} + r_e)}{(3r_{on1} + R_L)(r_{on2} + r_d + r_e) + (r_{on2} + r_e)r_d}\ ;$ $i_{C1} = \dfrac{V_{dc} - v_C - r_{on2} i_L}{(2r_{on2} + r_e)}\ ;\ i_{C2} = \dfrac{V_{dc} - V_d - v_C - r_d i_L}{(r_{on2} + r_e + r_d)}$
EC 2	$i_L = \dfrac{2v_C(r_{on2} + r_d + r_e) + 2(V_{dc} - V_d - v_C)(r_{on2} + r_e)}{(3r_{on1} + R_L)(r_{on2} + r_d + r_e) + 2(r_{on2} + r_e)r_d};$ $i_{C1} = 0\ ;\ i_{C2} = \dfrac{V_{dc} - V_d - v_C - r_d i_L}{(r_{on2} + r_e + r_d)}$
EC 3	$i_L = \dfrac{[3v_C(r_{on2} + r_d + r_e)(2r_{on2} + r_e) + (V_{dc} - V_d - v_C)}{(3r_{on1} + 2r_e + R_L)(r_{on2} + r_d + r_e) + (r_{on2} + r_e)r_d};$ $i_{C1} = \dfrac{V_{dc} - v_C - r_{on2} i_L}{(2r_{on2} + r_e)}\ ;\ i_{C2} = \dfrac{V_{dc} - V_d - v_C - r_d i_L}{(r_{on2} + r_e + r_d)}$
EC 4	$i_L = \dfrac{(V_{dc} + 3v_C)(r_{on2} + r_d + r_e) + (V_{dc} - V_d - v_C)(r_{on2} + r_e)}{(4r_{on1} + 2r_e + R_L)(r_{on2} + r_d + r_e) + (r_{on2} + r_e)r_d};$ $i_{C1} = 0\ ;\ i_{C2} = \dfrac{V_{dc} - V_d - v_C - r_d i_L}{(r_{on2} + r_e + r_d)}$
EC 5	$i_L = \dfrac{(V_{dc} + 4v_C)(2r_{on2} + r_e) + (V_{dc} - v_C)(r_{on2} + r_e)}{(4r_{on1} + 3r_e + R_L)(2r_{on2} + r_e) + (r_{on2} + r_e)r_{on2}};$ $i_{C1} = \dfrac{V_{dc} - v_C - r_{on2} i_L}{(2r_{on2} + r_e)}\ ;\ i_{C2} = 0$
EC 6	$i_L = \dfrac{2V_{dc} + 4v_C}{5r_{on1} + 4r_e + R_L}\ ;\ i_{C1} = 0\ ;\ i_{C2} = 0$

TABLE VI
INSTANTANEOUS AND AVERAGE CONDUCTION LOSSES FOR EQUIVALENT CIRCUITS OF PROPOSED 13 LEVEL SCMLI

EC 0	$p_0 = 2(2r_{on2} + r_e){i_{C1}}^2\ ;\ P_{ave,\,0} = \dfrac{4t_1}{T} p_0$
EC 1	$p_1 = 3r_{on1}{i_L}^2 + (2r_{on2} + r_e){i_{C1}}^2 + r_d(i_L + i_{C2})^2 + (r_{on2} + r_e){i_{C2}}^2;$ $P_{ave,\,1} = \dfrac{4(t_2 - t_1)}{T} p_1$
EC 2	$p_2 = 3r_{on1}{i_L}^2 + 2r_d(i_L + i_{C2})^2 + 2(r_{on2} + r_e){i_{C2}}^2;$ $P_{ave,\,2} = \dfrac{4(t_3 - t_2)}{T} p_2$
EC 3	$p_3 = (3r_{on1} + r_e){i_L}^2 + r_{on2}(i_L + i_{C1})^2 + r_d(i_L + i_{C2})^2$ $+(r_{on2} + r_e)({i_{C1}}^2 + {i_{C2}}^2)\ ;$ $P_{ave,\,3} = \dfrac{4(t_4 - t_3)}{T} p_3$
EC 4	$p_4 = (4r_{on1} + 2r_e){i_L}^2 + r_d(i_L + i_{C2})^2 + (r_{on2} + r_e){i_{C2}}^2\ ;$ $P_{ave,\,4} = \dfrac{4(t_5 - t_4)}{T} p_4$
EC 5	$p_5 = (4r_{on1} + 3r_e){i_L}^2 + r_{on2}(i_L + i_{C1})^2 + (r_{on2} + r_e){i_{C1}}^2;$ $P_{ave,\,5} = \dfrac{4(t_6 - t_5)}{T} p_5$
EC 6	$p_6 = (5r_{on1} + 4r_e){i_L}^2\ ;\ P_{av,\,6} = \dfrac{4(T/4 - t_6)}{T} p_6$

steady state voltage magnitude (v_c) (iii) both diodes have same internal resistance(r_d) and forward voltage drop (V_d).

With these assumptions, the proposed SCMLI has 7 equivalent circuits (ECs) corresponding to 7 magnitude of voltage levels (i.e. 0, ± $1V_{dc}$, ± $2V_{dc}$, ± $3V_{dc}$, ± $4V_{dc}$, ± $5V_{dc}$, ± $6V_{dc}$) as shown in Table IV. Where i_L presents load current, i_{c1} depicts charging current for either C_{11} or C_{21} and i_{c2} depicts charging current for either C_{12} or C_{22}.

By using KVL, the i_L, i_{c1} and i_{c2} for different ECs are evaluated and tabulated in Table V. The instantaneous conduction losses for an EC (p_i, i=0 to 6) can be evaluated by finding the ohmic losses associated with each internal resistance as shown in Table VI. As positive and negative half-cycles of output voltage waveform are symmetrical to each other, the conduction losses associated with a positive voltage level is same that for negative voltage level. Hence, the average conduction losses per output cycle for an EC ($P_{ave,i}$, i=0 to 6) can be evaluated by multiplying the corresponding p_i with a time ratio factor as shown in Table VI.

The time ratio factor can be calculated for a particular magnitude of voltage level. For example, for ± $1V_{dc}$, the total time duration per cycle is $4(t_2\text{-}t_1)$ as shown in Fig. 8. Hence time ratio factor is $4(t_2\text{-}t_1)$/T.

The overall conduction losses of proposed SCMLI is the summation of average conduction losses occurred in each EC. It can be evaluated by (18).

$$P_{con} = \sum_{j=0}^{6} P_{ave,\ j} \tag{18}$$

B. Analysis of switching losses

When a switch becomes on state from off state or becomes off state from on state, it will take some times namely t_{on} and t_{off} respectively. These times are called switching times. During these switching times, there exists some power losses in the switch which is known as switching losses. The switching losses can be evaluated over a fundamental cycle. For this, the number of switching transitions per cycle for a switch needs to be calculated. Considering linear variation of switch voltage and current during the switching times, the occurred energy losses in k^{th} switch can be evaluated by (19) and (20).

$$E_{k,on} = \int_0^{t_{on}} V_{swk}\left(1-\frac{t}{t_{on}}\right) I_k\left(\frac{t}{t_{on}}\right) dt = \frac{1}{6} V_{swk}\ I_k t_{on} \tag{19}$$

$$E_{k,off} = \int_0^{t_{off}} I_k'\left(1-\frac{t}{t_{off}}\right) V_{swk}\left(\frac{t}{t_{off}}\right) dt = \frac{1}{6} V_{swk}\ I_k' t_{off} \tag{20}$$

Where I_k and I_k' are current through the switch after it becomes on and before it becomes off respectively. Let, the number of on and off transitions per cycle for k^{th} switch are $N_{on,k}$ and $N_{off,k}$, the energy losses per cycle and the switching power losses for k^{th} switch can be evaluated by (21) and (22) respectively. The overall switching losses is the summation of all the individual switching losses which is expressed by (23).

$$E_{k,sw} = (N_{on,i} \times E_{i,on}) + (N_{off,i} \times E_{i,off}) \tag{21}$$

$$P_{k,sw} = \frac{(N_{on,k} \times E_{k,on}) + (N_{off,k} \times E_{k,off})}{T} = \frac{1}{6T} V_{swk} I_k (N_{on,k} t_{on} + N_{off,k} t_{off}) \tag{22}$$

$$P_{sw} = \sum_{k=1}^{14} P_{k,sw} \tag{23}$$

C. Analysis of capacitor voltage ripple losses

Due to the voltage difference between input supply voltage (V_{dc}) and capacitor voltage (v_c), the capacitor ripple losses occur. For evaluating ripple losses, the maximum voltage ripple of capacitor needs to be evaluated [**16-17**]. The expression for voltage ripple for a capacitor C_p can be presented by (24). Where $i_{Cp}(t)$ is the capacitor current when the capacitor is in discharging mode. The time duration (t_{k+1} - t_k) is the maximum discharging time period of capacitor C_p.

$$\Delta v_{Cp} = \frac{1}{C_p} \int_{t_k}^{t_{k+1}} i_{Cp}(t)\ \ dt \tag{24}$$

The capacitor voltage ripple losses per cycle for C_p can be presented by (25). From (25) it can be observed that the larger value of capacitance C_P reduces capacitor voltage ripple losses. In the proposed 13 level SCMLI, capacitor ripple losses for individual capacitor can be evaluated by (25). Therefore, overall capacitor ripple losses for proposed 13 level SCMLI can be presented by (26).

$$P_{ripCp} = \frac{1}{2T} C_p (\Delta v_{Cp})^2 = \frac{1}{2TC_p} \left(\int_{t_k}^{t_{k+1}} i_{Cp}(t)\ \ dt \right)^2 \tag{25}$$

$$P_{rip} = P_{ripC11} + P_{ripC12} + P_{ripC21} + p_{ripC22} \tag{26}$$

VIII. Comparison Study

The proposed SCMLI structure [PT] is compared with the recently developed SCMLIs presented in [**17, 20-27**]. As all the suggested topologies do not possess the same boosting factor (B) and same output voltage level (N_L), a cost comparison study is presented. Based on a cost function (CF) [**23-24**] and boosting factor (B) as shown in (27) and (28) respectively, CF per level per boosting factor ($CF/(N_L \times B)$) is evaluated for all the SCMLIs as shown in Table VII and VIII. Where α presents the weightage of the TSV.

$$CF = \left(N_{sw} + N_{dr} + N_d + N_{cap} + \alpha TSV_{pu}\right) \times N_{dc} \tag{27}$$

$$B = \frac{v_{o\max}}{\sum_{i=1}^{N_{dc}} V_{ini}} \tag{28}$$

Table VII presents the comparison study among the SCMLIs for symmetric dc source configuration. From this table, it can be observed that the PT[n=2] requires minimum components to produce 13 output voltage levels as compared to the structures presented in [**17, 22, 24-27**]. The structures presented in [**17, 20, 22-23, 25-26**] have lower boosting factor than PT. Further, structure in [**20**] requires 4 dc sources to produce 17 level output voltage whereas the PT with 2 dc sources can produce 13[n=2] and 17[n=3] levels output voltage.

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TABLE VII
COMPARISON STUDY OF PROPOSED SCMLI WITH OTHER SCMLIS WITH SYMMETRIC DC SOURCE CONFIGURATION

SCMLI	N_L	N_{dc}	N_{sw}	N_{dri}	N_{dio}	N_{cap}	N_{path}	N_{path_C}	B	TSV_{pu}	$CF/(N_L \times B)$	
											$\alpha = 0.5$	$\alpha = 1.5$
[17], 2014	13	3	18	18	3	3	9	2	2	5	5.13	5.71
[20], 2016	17	4	20	20	4	4	10	2	2	5	5.94	6.52
[22], 2018	13	3	18	18	6	6	9	2	2	4	5.76	6.23
[23], 2018	17	2	18	14	2	4	5	2	2	5	2.38	2.67
[24], 2019	13	2	16	16	-	4	7	3	3	5.6	1.99	2.27
[25], 2018	13	3	21	21	12	6	9	5	2	4.5	7.18	7.70
[26], 2019	13	2	20	16	-	6	6	5	1.5	5.3	4.57	5.12
[27], 2019	13	2	16	16	4	4	8	2	3	5.3	2.18	2.45
PT	13(n=2, *m*=1)	2	14	14	2	4	5	2	3	6	1.89	2.20
	17(n=3, *m*=1)	2	18	18	2	6	5	2	4	7.25	1.40	1.61

TABLE VIII
COMPARISON STUDY OF PROPOSED SCMLI WITH OTHER SCMLIS WITH ASYMMETRIC DC SOURCE CONFIGURATION

SCMLI	N_L	N_{dc}	N_{sw}	N_{dri}	N_{dio}	N_{cap}	N_{path}	N_{path_C}	B	TSV_{pu}	$CF/(N_L \times B)$	
											$\alpha = 0.5$	$\alpha = 1.5$
[17], 2014	25	2	12	12	2	2	9	2	2	5	1.220	1.420
[20], 2016	17 (*n*=1, *m*=1)	2	10	10	2	2	5	2	2	5	1.039	1.852
	49(*n*=2, *m*=1)	2	16	16	2	4	8	4	4	6	0.418	0.479
[21], 2016	17	2	10	10	2	2	5	2	2	5	1.039	1.852
	49	3	14	14	3	3	10	2	2	5	1.117	1.270
[23], 2018	49	2	18	14	2	4	5	2	2	6	0.836	0.959
[24], 2019	31	2	16	16	-	4	7	3	3	5.6	0.834	0.954
[25], 2018	25	2	14	14	8	4	6	5	2	4.5	1.690	1.87
[26], 2019	49	2	20	16	-	6	6	5	1.5	5.3	1.214	1.359
PT	31(*n*=2, *m*=1)	2	14	14	2	4	5	2	3	6	0.795	0.924
	49(*n*=3, *m*=1)	2	18	18	2	6	5	2	4	7.25	0.465	0.539

The proposed structure has the minimum $CF/(N_L \times B)$ as compared to others. The topology presented in [**23**] can produce 17 levels with a $CF/(N_L \times B)$ of 2.38(α=0.5) and 2.67(α=1.5) whereas the proposed structure can produce 17 level output voltage with $CF/(N_L \times B)$ of 1.40(α=0.5) and 1.61(α=1.5). Further, the variation of $CF/(N_L \times B)$ w.r.t N_L is shown in Fig. 10. It can be observed that PT[*n*=3] provides the lowest $CF/(N_L \times B)$ among all suggested topologies and PT[*n*=2] provides the lower $CF/(N_L \times B)$ as compared to the topologies presented in [**17, 20, 24-27**].

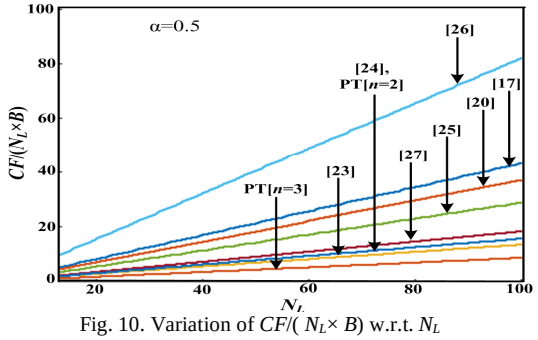

Fig. 10. Variation of $CF/(N_L \times B)$ w.r.t. N_L

Table VIII shows the comparison study of PT with others for asymmetric dc source configuration. From this table, it can be observed that PT can produce 31 output voltage levels using lower number of switches and drivers as compared to the SCMLI presented in [**24**]. SCMLIs presented in [**17**] and [**25**] can produce 25 output voltage levels using 12 and 14 switches respectively and 2 dc sources of magnitude V_{dc} and $5V_{dc}$ whereas the proposed structure can produce 31 output voltage levels using 14 switches with 2 dc sources of magnitude V_{dc} and $4V_{dc}$. Hence, relatively lower number of switches are required for producing higher voltage levels in proposed SCMLI as compared to [**17**] and [**25**]. Further, SCMLIs presented in [**23**] and [**26**] can produce 49 output voltage levels using 18 and 20 switches with 2 dc sources of magnitudes ($2V_{dc}$, $10V_{dc}$) and (V_{dc},$7V_{dc}$) respectively whereas the proposed SCMLI can produce 49 output voltage levels using 18 switches with 2 dc sources of magnitudes (V_{dc} , $5V_{dc}$). Hence, as compared to [**23**] and [**25**], the proposed structure requires lower magnitude of dc sources and comparatively cost of the PT is lower than [**23**] and [**25**].

The SCMLIs presented in [**20-21**] can produce 17 levels using 10 switches using 2 dc sources of V_{dc} and $3V_{dc}$. Hence the switch per level is (10/17)=0.588 whereas the proposed topology can produce 31 levels using 14 switches i.e. switch per level (14/31)=0.451. However the SCMLI presented in [**20**] requires lower switches and drivers for generating higher voltage levels as compared to the proposed SCMLI. For example, for 49 level generation, the SCMLI in [**20**] requires 16 switches and 16 drivers and 2 dc sources of magnitude V_{dc} and $5V_{dc}$ whereas the proposed topology requires 18 switches, 18 drivers and 2 dc sources of magnitude V_{dc} and $5V_{dc}$. But the

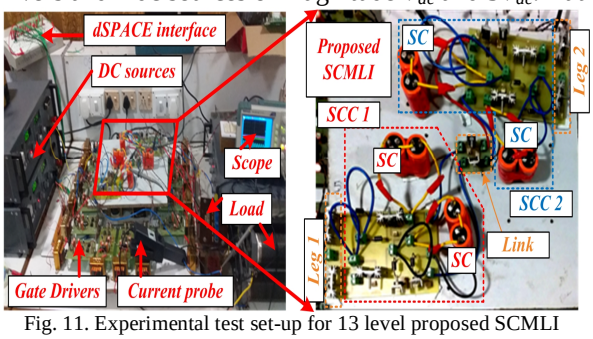

Fig. 11. Experimental test set-up for 13 level proposed SCMLI

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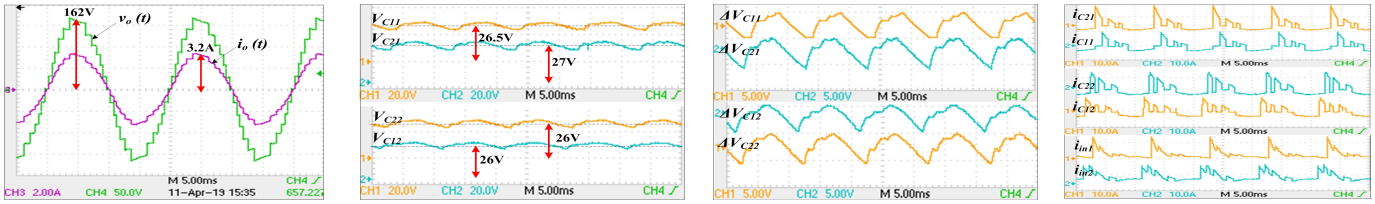
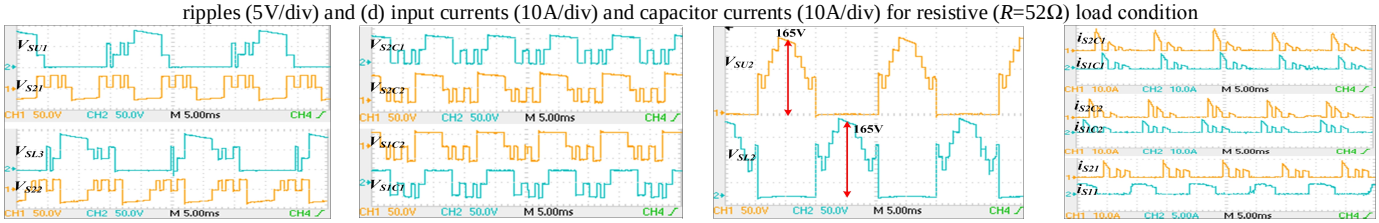


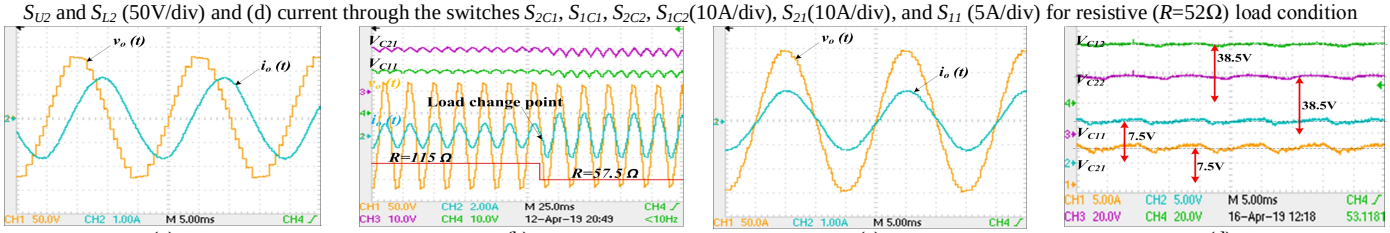
(a) (b) (c) (d)

Fig.12. Experimental waveforms for (a) 13 level output voltage and output current (50V/div and 2A/div), (b) capacitor voltages (20V/div), (c) capacitor voltage ripples (5V/div) and (d) input currents (10A/div) and capacitor currents (10A/div) for resistive (R=52Ω) load condition



(a) (b) (c) (d)

Fig.13. Experimental waveforms for (a) stress voltage for S_{U1}, S_{21}, S_{L3} and S_{22} (50V/div) (b) stress voltage for S_{2C1}, S_{2C2}, S_{1C2}, S_{1C1} (50V/div)(c) stress voltage for S_{U2} and S_{L2} (50V/div) and (d) current through the switches S_{2C1}, S_{1C1}, S_{2C2}, S_{1C2}(10A/div), S_{21}(10A/div), and S_{11} (5A/div) for resistive (R=52Ω) load condition



(a) (b) (c) (d)

Fig.14. Experimental waveforms for (a) 13 level output voltage and output current (50V/div and 2A/div) for R-L (R=41Ω and L=150mH) load condition, (b) output voltage and current with capacitor voltages for dynamic load condition (c) 31 level output voltage (50V/div) and output current (1A/div) for resistive (R=125Ω) load condition (d) capacitor voltages for asymmetric sources (V_{in1}=10V and V_{in2}=40V)

SCMLI in [**20**] requires more variety of capacitors with different voltage rating as compared to proposed SCMLI. Although the SCMLI presented in [**21**] requires lower switches and drivers for producing higher voltage level as compared to the proposed topology, the structure in [**21**] cannot add all the dc sources which increases the number of dc source requirement as compared to proposed one as shown in Table VIII. As per Table VIII, it can be observed that except the 49 level structure of [**20**], the proposed topology requires lower $CF/(N_L \times B)$ as compared to others. Further, the proposed topology requires lowest N_{path} and N_{path_C} as compared to others which improves the capacitor voltage and output voltage profiles.

IX. Experimental Results

For experimental study, proposed structure with n=2 and m=1 is developed as shown in Fig. 11. The input sources are selected as 30V each for symmetrical study and 10V and 40V for asymmetrical study. IRF 640 (MOSFET) is considered as the switching device for all the switches those have anti-parallel diode. Further, the switches those do not have anti-parallel diode, are implemented by connecting a series diode (MUR 460) with IRF 640. The switching pulses are generated by dSPACE 1104 controller. All the SCs have equal capacitance of 2500μF (Considering 3.2A peak load current and R_L=52Ω).

Fig.12(a) shows the experimental waveform of 13 level output voltage ($v_o(t)$) and load current ($i_o(t)$) for resistive load (R_L=52Ω) condition. From FFT analysis, it is observed that the fundamental peak magnitude and THD of $v_o(t)$ and $i_o(t)$ are (162.1V, 7.45%) and (3.21A, 6%) respectively. The experimental output power is 260W. Further, under this load condition, the efficiency of the inverter is 91.06% (conduction losses=20W, switching losses=10mW and capacitor ripple losses=5.5W). Under this load condition, the capacitor voltages are shown in Fig. 12(b). It can be observed that the capacitor voltages are well balanced with the proposed switching table (Table III). Fig. 12(c) depicts the capacitor voltage ripples for this same load conditions. It can be observed that the capacitor voltage ripples are within 5V to 6V (within 16.67% to 20% of 30V). Under this same load condition, the capacitor currents and input source currents are observed and are shown in Fig. 12(d). It can be observed that the currents are pulsating in nature due to the charging state of the capacitors.

Under this load condition, the stress voltage for different switches are shown in Fig. 13. Fig. 13(a) shows the stress voltage for the switches S_{U1}, S_{21}, S_{L3} and S_{22}. The maximum stress voltage of S_{U1}, S_{21}, S_{L3} and S_{22} are 85V, 26V, 85V and 26V respectively. The maximum stress voltage for S_{2C1}, S_{2C2}, S_{1C2} and S_{1C1} are within 60V, 26V, 60V and 26V respectively as shown in Fig. 13(b). Similarly, the maximum stress voltages for the switches S_{U2} and S_{L2} are within 165V as depicted in Fig. 13(c). Fig. 13(d) shows the current stress of switches S_{2C1}, S_{2C2}, S_{1C1}, S_{1C2}, $S_{21}$and S_{11}. The maximum current stress of these switches are within 10A.

Further, the 13 level inverter structure is experimentally verified for R-L (R=41Ω and L=150mH)and dynamic load conditions with considering 20V dc sources. Fig. 14(a) shows

the output voltage and current waveforms for *R-L* load condition. It can be observed that the load current lags the output voltage due to the inductive nature of the load. For testing dynamic load condition, the inverter is initially loaded with high resistive load (R=115Ω) , after some time the load resistance is decreased to half of initial value (i.e. R=57.5Ω). With this sudden load change, the output voltage, load current, capacitor voltages are observed and are shown in Fig. 14(b). It can be observed that the capacitor voltages remains stable within the specified 20V range after the load change point.

The proposed SCMLI is verified for asymmetric dc source configuration (V_{in1}=10V and V_{in2}=40V) with resistive load (R=125Ω) condition. The 31 level output voltage with load current and capacitor voltages are shown in Fig. 14(c) and 14(d) respectively.

X. Conclusion

In this paper, a SCC structure with reduced components has been proposed first. The operating principle of BC of proposed SCC has been discussed. Further, the generalized SCC has been developed. After that SCMLI structure using 2 SCCs is developed and the extended form of proposed SCMLI has been presented. The detail analysis of capacitor selection procedure for 13 level SCMLI has been presented. A detail comparison study shows that the proposed SCC and SCMLI structures require lower components, N_{path} and N_{path_C} for producing a output voltage level as compared to recently developed SCCs and SCMLIs. Further, the proposed SCMLI provides lowest $CF/(N_L \times B)$ among all the suggested topologies. Considering, fundamental switching frequency scheme, extensive experimental results have been presented for verifying the merits and effectiveness of the proposed structures.

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